

## FEATURES

## CFEC\_12000x8 400/200G Custom Protocol RSFEC Version 1.1

### SUPPORTED STANDARDS

- IEEE 802.3bj-2014
- IEEE 802.3by d1p0
- IEEE 802.3bx d3p0
- IEEE 802.3bs pre-draft

### IP DETAILS

- Performs the encoding and decoding of a 5140-bit message using RS (544,514) and RS (528,514) over multiple SerDes lanes.
- 1x400G KP RSFEC (544,514) over 8x50G SerDes
- 1x400G KR RSFEC (528,514) over 8x50G SerDes
- 2x200G KP RSFEC (544,514) over 4x50G SerDes
- 2x200G KR RSFEC (528,514) over 4x50G SerDes

### DELIVERABLES

- Synthesizable custom configured RTL, documentation, sample synthesis and STA scripts, verification report.

### APPLICATIONS

- Ethernet

### INTRODUCTION

The CFEC\_12000x8 is a custom protocol Reed Solomon Forward Error Correction encoder/decoder block designed to replicate the 400G Ethernet functions for a datastream based on unscrambled 128b/130b blocks. This block performs the encoding and decoding of a 5140-bit message using the RS (544,514) and RS (528,514) defined in the IEEE 802.3bj-2014 Ethernet Standard.

The CFEC\_12000x8 is designed for synchronous operation over a single clock domain of minimum 781.25 Mhz, there is no functional maximum speed limit for the clock. Rate modulation is done through a backpressured tx rdy/rx vld scheme

### FUNCTIONALITY

The CFEC\_12000x8 performs the following functions:

- Transcoding (128b/130b to 256b/257b)
- Scrambling
- Alignment Insertion/Removal (802.3bs style alignment markers)
- Parity Generation
- Decoding/Error Correction

The user must integrate the following components in their own external logic:

- Alignment Lock
- Deskew
- Lane Remapping
- Async FIFOs

The IP contains the following features:

### ERROR INDICATION

Any codeword with detected errors exceeding the correctable limit will be indicated as errored on output. The correctability of a codeword is computed before the codeword is sent to upper layer of logic to prevent any errors from propagating. Error indication is performed using by corrupting the sync headers of the 64/66 blocks after transcoding.

### CORRECTION/INDICATION BYPASS (LOW LATENCY)

Depending on the application and link quality it may be desirable to disable the Error Indication and/ or the Error Correction function to reduce latency. The following four modes are supported:

- Normal Operation: Codewords are corrected and any uncorrectable errors are indicated.
- Fast Correct: If the application can reliably detect corrupted data, then the error indication can be bypassed to reduce decoding time. It is possible that the decoder will attempt to and fail to correct an uncorrectable codeword, corrupting it further.
- Indication Only: Used if the link quality requires no gain, but the application requires a strong parity checking mechanism to ensure data quality.
- Cut through: Allows protocol compatible traffic to be sent/received but incurs no latency from decoding the codeword.

Additionally multiple interrupts, event triggers and statistics counters are available.



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