FEATURES

CMC400_58AA Universal 400G Ethernet MAC/PCS/FEC

SUPPORTED STANDARDS

- IEEE 802.3-2018
- Consortium 25/50G
- USXGMII

IP DETAILS

- Total bandwidth of 400G
- Maximum of 8 Channels
- 400GbE - 10GbE
- 4 or 8 or 16 SerDes Lanes
- 100G or 50G or 25G SerDes
- 512bit / 800Mhz operation
- RS (544, 514) FEC
- RS (528, 514) FEC
- Firecode FEC
- Pause Frame Support
- Priority Flow Contol
- AXI Register interface
- FIFO Application Interface
- RMON Statistics
- Jumbo Frames up to 16k
- QinQinQ VLAN Tags
- FCS Offload and Checking
- Runt Frame Padding
- 2-Step PTP
- SERDES Remapping
- Energy Efficient Ethernet
- Deficit Idle Counter

DELIVERABLES

- RTL (System Veriilog)
- Synthesis Contraints
- Documentation
- Sample Testbench

APPLICATIONS

- High Speed Switching
- Data Center

INTRODUCTION

The UMAC (CoMira's Universal Ethernet MAC) is a low latency, low area, channelized multi-speed MAC-PCS-FEC core handling all Ethernet functions from OSI Layer 2 down to the SerDes (PMD). The multi-speed / multi-channel nature of the core allows it to support mixtures of PHY speeds simultaneously, with each channel being controlled and reported independently.

Channel	Mode	SERDES	FEC
Ch 0	400G-R8	8x50G (PAM4)	RS(544,514)
Ch 0 Ch 4	200G-R4 100G-R4 40G-R4	4x50G (PAM4) 4x25G (NRZ) 4x10G (NRZ)	RS(544,514) RS(528,514)
Ch 0,2 Ch 4,6	100G-R2 50G-R2	2x50G (PAM4) 2x25G (NRZ)	RS(544,514) RS(528,514)
Ch 0-7	25G-R 10G-R USXGMII	1x25G (NRZ) 1x10G (NRZ) 1x10G (NRZ)	RS(528,514)

MEDIA ACCESS CONTROLLER (MAC)

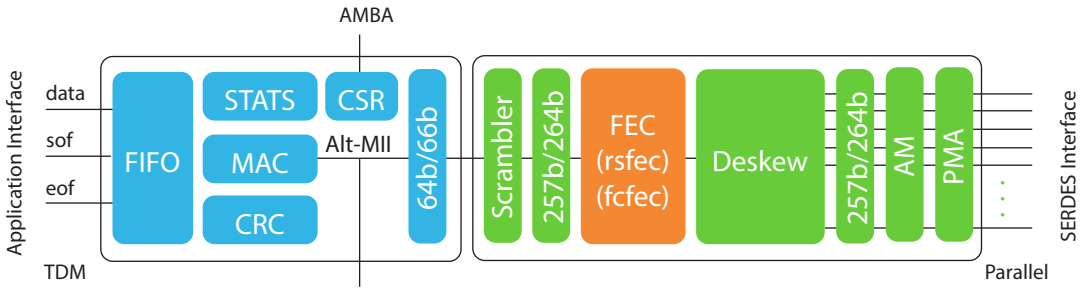
The UMAC Layer 2 MAC is an Ethernet MAC performing the function of Clause 3 in the IEEE 802.3 standard. The MAC performs the framing operations needed to encapsulate data for use in an ethernet network such as FCS / preamble insertion, and handling Layer 2 flow control via pause frames. The MAC is a cut through configuration supporting a minimum data dwell time, where packets may start sending before they are fully queued. The MAC has full support for RMON statistics and can handle runts and jumbo frames.

PHYSICAL CODING SUBSYSTEM (PCS)

The PCS handles the necessary functions to put a packet on the wire and receive it without errors. Encoding/Decoding using 8b/10b, 64b/66b, 264b/257b to allow overhead in the data. Scrambling to provide sufficient transitions in the SerDes and alignment marker insertion / deskewing to align and recombine data from multiple serdes lanes into one channel.The PCS operates in a bit transparent mode that enables applications in Optical Transport Networks, Flexible Ethernet, MLG, as well as other PHY types such as FibreChannel and various encapsulations of other non-Ethernet standards.

FORWARD ERROR CORRECTION (FEC)

The FEC provides the gain needed to allow long transmission distances and high SerDes speeds. The FEC is a tradeoff between coding gain and added latency, a high gain Reed Solomon (544,514) correcting 15x10bit symbols being used for 56G PAM4 SerDes, Reed Solomon (528,514) correcting 7x10bit symbols used for 25G NRZ SerDes and FireCode (2112,2080) correcting 11x1bits for 10G NRZ SerDes. The error correction rates and status are tracked and reported via the clause 45 counters and registers.



ADDRESS
40087 Mission Blvd,
#388 Fremont, CA 94539

PHONE
408.418.8235
WEBSITE
www.comira-inc.com